

(FILE 'USPAT' ENTERED AT 16:03:47 ON 20 DEC 94)

L1 391449 S COMPRESS?
L2 24226 S L1 AND MEMORY
L3 21219 S ONE(W)BIT
L4 457 S L1(P)L3
L5 360 S L4 AND L2
L6 8 S L5 AND 365/CLAS
L7 921782 S READ?
L8 34937 S L1(P)L7
L9 93 S L8 AND 365/CLAS
L10 3 S L9 AND 365/201/CCLS
L11 11 S L9 AND WIRED

=> d 110 1-3

~~1. 5,313,424, May 17, 1994, Module level electronic redundancy; Robert D. Adams, et al., **365/200**, **96**, **201**, **210** [IMAGE AVAILABLE]~~

~~2. 5,148,398, Sep. 15, 1992, Semiconductor memory device with built-in test circuit and method for testing the same; Tohru Kohno, **365/201**; 371/21.1 [IMAGE AVAILABLE]~~

~~3. 4,918,378, Apr. 17, 1990, Method and circuitry for enabling internal test operations in a VLSI chip; Haluk Katircioglu, et al., **365/201**; 371/21.2, 22.4, 22.5 [IMAGE AVAILABLE]~~

=> d 16 1-8

~~1. 5,357,475, Oct. 18, 1994, Method for detaching sectors in a flash EEPROM **memory** array; Robert N. Hasbun, et al., **365/218**, **200**; 371/10.1, 10.2, 11.1, 21.1; 395/575 [IMAGE AVAILABLE]~~

~~2. 5,341,339, Aug. 23, 1994, Method for wear leveling in a flash EEPROM **memory**; Steven E. Wells, **365/218**, **185**, **900** [IMAGE AVAILABLE]~~

~~3. 5,337,275, Aug. 9, 1994, Method for releasing space in flash EEPROM **memory** array to allow the storage of **compressed** data; Richard P. Garner, **365/189.01**, **230.01**, **900** [IMAGE AVAILABLE]~~